Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) A method of ~~preparing a wafer for~~ fabricating an integrated circuit ~~fabrication~~ device comprising:

providing a bulk silicon substrate;

depositing a carbon-doped silicon layer on said bulk silicon substrate; ~~and~~

growing an epitaxial silicon layer overlying said carbon-doped silicon layer to provide a starting wafer for integrated circuit fabrication; and

fabricating said integrated circuit device on said starting wafer by the steps comprising:

forming a gate electrode on said starting wafer;

implanting LDD and source and drain regions within said epitaxial silicon layer adjacent to said gate electrode; and

implanting a heavy ion to form halo implants within said epitaxial silicon layer adjacent to said LDD regions and underlying said gate electrode wherein said halo implants extend to an interface between said epitaxial silicon layer and said carbon-doped silicon layer.

2. (original) The method according to Claim 1 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

3. (original) The method according to Claim 1 wherein said carbon-doped silicon layer has a thickness of between about 100 and 200 Angstroms.

4. (currently amended) The method according to Claim 1 wherein said carbon-doped silicon layer has a carbon content of up to 0.5% atomic percent.

5. (original) The method according to Claim 1 wherein said epitaxial silicon layer has a thickness of between about 300 and 400 Angstroms.

6. (currently amended) A method of fabricating an integrated circuit device comprising:

providing a bulk silicon substrate;

depositing a carbon-doped silicon layer on said bulk silicon substrate;

growing an epitaxial silicon layer overlying said carbon-doped silicon layer to provide a starting wafer for said integrated circuit device fabrication; and

fabricating said integrated circuit device on said starting wafer by the steps comprising:

forming a gate electrode on said starting wafer;

implanting LDD and source and drain regions in said starting wafer adjacent to said gate electrode; and

implanting ~~a~~ antimony or indium ~~heavy~~ ions within said epitaxial silicon layer to form halo implants adjacent to said LDD regions and underlying said gate electrode wherein said halo implants extend to an interface between said epitaxial silicon layer and said carbon-doped silicon layer.

7. (original) The method according to Claim 6 wherein said carbon-doped silicon layer is deposited by chemical vapor deposition.

8. (original) The method according to Claim 6 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

9. (original) The method according to Claim 6 wherein said carbon-doped silicon layer has a thickness of between about 100 and 700 Angstroms.

10. (currently amended) The method according to Claim 6 wherein said carbon-doped silicon layer has a carbon content of up to 0.5% atomic percent.

11. (original) The method according to Claim 6 wherein said epitaxial silicon layer has a thickness of between about 300 and 500 Angstroms.

12. (original) The method according to Claim 6 wherein carbon ions in said carbon-doped silicon layer act as a silicon interstitial sink for silicon interstitials formed by said halo implants to prevent end of range secondary defect formation.

13. (canceled)

14. (currently amended) A method of fabricating an integrated circuit device comprising:

providing a bulk silicon substrate;

depositing a carbon-doped silicon layer on said bulk silicon substrate;

growing an epitaxial silicon layer overlying said carbon-doped silicon layer to provide a starting wafer for said integrated circuit device fabrication; and

fabricating said integrated circuit device on said starting wafer by the steps comprising:

forming a gate electrode on said starting wafer;

implanting LDD and source and drain regions ~~in said starting wafer~~ within said epitaxial silicon layer adjacent to said gate electrode; and

implanting heavy ions to form halo implants within said epitaxial silicon layer adjacent to said LDD regions and underlying said gate electrode wherein said halo implants extend to an interface between said epitaxial silicon layer and said carbon-doped silicon layer wherein carbon ions in said carbon-doped silicon layer act as a silicon interstitial sink for silicon interstitials formed by said halo implants to prevent end of range secondary defect formation.

15. (original) The method according to Claim 14 wherein said carbon-doped silicon layer is deposited by reduced pressure chemical vapor deposition.

16. (original) The method according to Claim 14 wherein said carbon-doped silicon layer has a thickness of between about 100 and 700 Angstroms.

17. (currently amended) The method according to Claim 14 wherein said carbon-doped silicon layer has a carbon content of up to 0.5% atomic percent.

18. (original) The method according to Claim 14 wherein said epitaxial silicon layer has a thickness of between about 300 and 500 Angstroms.

19. (original) The method according to Claim 14 wherein said heavy ions comprise antimony or indium.

20-25. (canceled)

26. (new) The method according to Claim 1 wherein carbon ions in said carbon-doped silicon layer act as a silicon interstitial sink for silicon interstitials formed by said halo implants to prevent end of range secondary defect formation.

27. (new) The method according to Claim 1 wherein said heavy ions comprise antimony or indium.